Amendments to the Specification:

Please replace the paragraph beginning on page 5, line 3, with the following rewritten paragraph:

The integrated ~~circuit~~ circuit 1 represented in figure 1 comprises several subassemblies 2 (five subassemblies 2a to 2e in figure 1). The subassemblies each comprise a first power supply terminal B1, a second power supply terminal B2 and a clock input, respectively H1 to H5. The subassemblies are connected in series, by means of their power supply terminals B1 and B2, to the terminals of a voltage supply source 3, connected in parallel with a decoupling capacitor 4. The same current, noted I, flows through the different subassemblies. The clock inputs H1 to H5 of the subassemblies 2a to 2e are connected to a common clock circuit 5 by means of devices 6,7 for shifting the clock signal levels. Shifting the clock signal levels consists in applying clock signals to the different subassemblies 2, the voltage level of which signals is adapted to the different supply voltages present at the terminals B1 and B2 of the different subassemblies 2. This does not, as in certain known systems, merely involve applying a single clock signal to different circuits of the system, supplied in parallel or independent manner (see in particular US 5,486,783). The voltage shift of the tension clock signal levels is necessary to compensate the potential differences dues to power supply of the different subassemblies 2 in series.